filling said contact with a conducting material.

Remarks

Claims 21-32, 35, 36, 40-43, and 48 are pending in the application. Claims 26-30, 35, 36, 40-43 and 48 have been withdrawn from consideration in response to a restriction requirement. Claims 21-25, 31 and 32 have been rejected.

Claims 31-32 have been rejected under 35 USC §112, first paragraph. Claim 31 has been amended to overcome the 35 USC §112, first paragraph rejection by following the Examiner's suggestion of reordering the steps of recitation and by clarifying the reordered step. Claim 32 was rejected as being dependent upon a rejected base claim. Claims 31 and 32 are now in compliance with 35 USC §112, first paragraph.

Claims 21-24 and 31-32 have been rejected under 35 USC § 102(e) as being anticipated by Zamanian (U.S. Patent No. 5,793,111). Zamanian teaches a semiconductor integrated circuit having an improved landing pad. Referring to Fig. 6, Zamanian teaches an oxide layer 28 that includes an opening 30 formed through the oxide layer 28. A polysilicon layer 32 is formed over the oxide layer 28 and the contact opening 30. A silicide layer 36 is formed over the polysilicon layer 32. A barrier layer 34 is formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are formed, wherein barrier layer 34 is located in the bottom of the contact opening underlying the aluminum layer 44. See col. 5 lines 49-63.

Applicants respectfully traverse this rejection as Zamanian does not teach every element of the invention as claimed in independent claims 21 and 31. Specifically, claims 21 and 31 recite that the contact is formed in said contact hole...**contacting** said vertical component. Zamanian teaches the bottom of the conductive contact 44 being either the silicide layer 36 or the barrier layer 34. See Fig. 5; Fig. 6; and col. 5, lines 61-63. The silicide layer 36, as shown in Fig. 5, or the barrier layer 34, as shown in Fig. 6, do not allow the conductive contact 44 to contact the vertical component of conductive

material 32 formed in the oxide layer 28. Thus, every element of independent claims 21 and 31 is not taught. Claims 22-24 depend from claim 21 and claim 32 depends from claim 31, therefore, applicants respectfully request that this rejection to claims 21-24 and 31-32 be withdrawn.

Claims 31-32 have been rejected under 35 USC § 102(e) as being anticipated by Okada et al. (U.S, Patent No. 5,399,890). Okado et al. teaches a semiconductor memory that includes an isolation region 2 and transistors 3a and 3b formed on a semiconductor substrate 1. A bit line 4 of a metal or silicide or polycide is formed on the semiconductor substrate on which a first interlayer insulating film 5 is deposited. Contact holes 6 and 6a are formed after which a conductive layer is formed. The conductive layer is patterned to form node electrode 7a and a first level interconnection layer 7b. A capacitance insulating film 8 is then formed over the node electrode 7a and the first level interconnection layer 7b. The capacitance insulating film 8 is etched to form a plate electrode 9. A second interlayer insulating film 10, formed of silicon oxide, is formed over the plate electrode 9. Contact holes 11 that reach designated regions of the plate electrode 9 and the first level interconnection layer 7b are opened through the second interlayer insulating film 10.

Applicant respectfully traverses the rejection as every element of the claimed invention is not taught by Okada et al. Okada et al. does not teach etching a contact hole in the overlayer and in an overetch amount of the substantially vertical component. Rather, Okada et al. teaches a contact 11 that is formed in the overlayer 10 that does not have an overetch amount of a substantially vertical component of the conductive layer. The contact 11 in Figs. 2C and 3 may touch the conductive layer, but the contact does not extent into the conductive layer.

Claims 21-25 and 31-32 have been rejected under 35 USC §103(a) as being unpatentable over Matsuo et al. (U.S. Patent No. 5,312,769) taken with Zamanian and Wolf pages 547-554. Matsuo et al. teaches a p-type silicon substrate having a n+-type diffused region formed in the silicon substrate 1, a gate oxide film 4 formed on the silicon

substrate, an insulting film 21, and a first interlayer insulating film 23 formed on the insulating film 21 covering first and second polycrystalline silicon lead pads 12 and 22. As indicated by the Examiner, the first interlayer insulating film 23 is not overetched when forming the contact hole. Zamanian is explained above. Wolf teaches a basic etching of silicon and silicon dioxide with fluorocarbon-containing plasma along with anisotropy etching. Wolf indicates that while etching SiO_2 the underlying Si layer may be etched, but not significantly. See page 549.

The Examiner asserts that it would have been obvious to form the contact hole of Matsuo et al by etching a contact hole in the overlayer insulator 23 and in an overetch amount of the layer 12 of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Wolf, wherein the contact is formed in the overlayer and in the vertical component. The Examiner reasons this is to insure that all of the dielectric of the overlayer has been completely removed from the contact hole providing a secure and good electrical connection from the layer of conductive material to the contact.

The Examiner admits that Matsuo et al. does not teach overetching the first interlayer insulating film 23 when forming the contact hole. Therefore, the Examiner relies upon the teachings of Zamanian and Wolf to cure this deficiency. Applicant respectfully traverses this rejection because the teaching of Wolf is not combinable with Zamanian due to the differences in their teaching of overetching. Wolf explains on page 549 that overetching of an underlying Si layer may be necessary, but the overetching does not significantly etch the Si layer. Zamanian on the other hand teaches at col. 6, lines 3-4 that overetching of a dielectric layer may etch away part or all of the barrier layer 34 in the opening. Thus, Wolf teaches an etching procedure where overetching may occur, but if it does occur, the overetching does not significantly affect the underlayer and is purely incidental. In contrast, Zamanian teaches that overetching of a dielectric layer is required and that a significant portion, if not all, of the barrier layer is removed. One of ordinary skill in the art would not combine Wolf with Zamanian because the two

references teach away from one another, i.e. Wolf teaches that significant overetch does not occur and Zamanian teaches that significant overetch does occur.

Finally the combination of Matsuo et al. with Zamanian and Wolf does not teach the claimed invention. The result of the combined teachings as suggested by the Examiner would be the contact hole of Mastuo et al. extending through the barrier layer of Zamanian possibly barely scratching the surface of the silicide layer, as taught by Wolf. Another possible result would be the contact hole of Mastuo et al. extending through the barrier layer and the silicide layer of Zamanian and, as taught by Wolf, possibly barely scratching the surface of the polysilicon layer of Zamanian. Neither result teaches or suggests the claimed invention. Specifically, the claimed invention teaches forming a contact in the contact hole that is **contacting** the vertical component, simply scratching the surface of the polysilicon layer would not contact the vertical component.

Claims 21-25 and 31-32 have been rejected under 35 USC §103 (a) as being unpatentable over Okada et al, taken with Zamanian, and Toshiyuki et al. (JP – 05-109905). The Examiner states that it would have been obvious to form the contact hole of Okada et al by etching a contact hole in the overlayer insulator and in an overetch amount of the layer of conductive material having a substantially vertical component, as taught by Zamanian and Toshiyuki, where a contact is formed in the overlayer and in the vertical component.

Toshiyuki et al. teaches etching of an insulting layer 3 to form an opening in the contact layer 2 and filling this contact layer 2 with an electrode layer 6. Applicants respectfully traverse this rejection because the reference teachings are not combinable. Specifically, there is no teaching or suggestion in Toshiyuki et al. to form an underlayer over a substrate that has a portion etched away creating a vertical component in the substrate and filling that portion with a conductive layer. In paragraph 0015, Toshiyuki et al teaches away from forming a vertical component in the substrate by stating that the 1st wiring layer 2 is placed on a base that is almost flat. Thus, one of ordinary skill in the

art would not combine Toshiyuki et al. with Zamanian or Okada et al. because Toshiyuki et al. teaches away from the methods taught by Zamanian and Okada et al.

Even if the reference teachings were combined, the present invention would not result. A combination of the references in the manner suggested by the Examiner would result in the contact hole of Okada et al. being formed in an overetched portion of the landing pad, the landing pad having a flat base over the substrate (as taught in Toshiyuki et al.), wherein the overetched portion is the barrier layer of Zamanian. This is not the invention as claimed.

In CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, L.L.P.

By Julie Cope
Julie G. Cope
Registration No. 48,624

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724

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